

IN THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit comprising:
a plurality of gate circuits; and
a control circuit configured to control the operation of some two or more gate circuits among said plurality of gate circuits, each of said some gate circuits among said plurality of gate circuits two or more gate circuits controlled by said control circuit, said control circuit including:

a logic circuit constituted by a plurality of first transistors; and
a switch circuit which includes second and third transistors controlled to turn on/off by said control circuit, each having a threshold voltage higher than that of each of said first transistors and conductive types different from each other, said switch circuit being capable of cut off said logic circuit from a power supply line by simultaneously turning off said second and third transistors;
wherein said some gate circuits two or more gate circuits controlled by the plurality of first transistors are provided on a critical path.

2. (Cancelled)

3. (Currently Amended) A logic operation semiconductor integrated circuit comprising:
a two or more gate circuits, which is each being connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and
a control circuit configured to control the operation of said two or more gate circuits;
and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors,

a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

4. (Original) A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 3 is provided on a critical path.

5. (Previously Presented) A logic operation circuit comprising:
a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of each of said first transistors; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of each of said first transistors,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa.

6. (Original) The logic operation circuit according to claim 5, wherein a source/drain terminal of said first transistor in said gate circuit is connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

7. (Original) A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 5 is provided on a critical path.

8. (Previously Presented) A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a storage circuit capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltages higher than that of each of said first transistors,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit.

9. (Currently Amended) The logic operation circuit according to claim 8, wherein a source/drain terminal of said first transistor in said gate circuit is connected to a source/drain terminal of another first transistor in said gate circuit, to said second reference voltage line circuit or an output terminal of said gate circuit.

10. (Original) A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 11 is provided on a critical path.

11. (Previously Presented) A logic operation circuit comprising:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than that of each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a bypass circuit which is connected to said gate circuit in parallel and constituted by a circuit substantially equal to said gate circuit by using a plurality of fourth transistors having a threshold voltage higher than that of each of said first transistors,

said bypass circuit being connected between said first and second reference voltage lines.

12. (Original) A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 11 is provided on a critical path.

13. (Original) A semiconductor integrated circuit, wherein said logic operation circuit defined in claim 11 is provided on a critical path.

14. (Currently Amended) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal, and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits includes each including:
~~a gate circuit which is connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors; and~~
~~a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors;~~

Circuit
~~a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit, and~~

~~said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits~~

two or more gate circuits, each being connected between a virtual voltage line and a first reference voltage line and constituted by a plurality of first transistors,

a control circuit configured to control the operation of said two or more gate circuits,
and

a second transistor which is connected between a second reference voltage line and said virtual voltage line and constituted by a transistor having a threshold voltage higher than that of each of said first transistors,

a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit or an output terminal of said gate circuit.

15. (Previously Presented) A flip flop comprising:

 a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits includes:

a gate circuit which is connected between a first reference voltage line and a virtual voltage line and constituted by a plurality of first transistors;

a second transistor which is connected between said virtual voltage line and a second reference voltage line and has a threshold voltage higher than that of each of said first transistors; and

a third transistor which is connected between said first reference voltage line and an output terminal of said gate circuit and has a threshold voltage higher than that of each of said first transistors,

said second and third transistors being on/off-controlled in such a manner that one of them is turned on while the other is turned off and vice versa, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

16. (Previously Presented) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or interception between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or interception between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit;

and a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits includes:

a gate circuit which is constituted by a plurality of first transistors and connected to first and second virtual voltage lines;

a second transistor which is connected between a first reference voltage line and said first virtual voltage line and has a threshold voltage higher than each of said first transistors;

a third transistor which is connected between a second reference voltage line and said second virtual voltage line and has a threshold voltage higher than that of each of said first transistors; and

a storage circuit capable of holding output logic of said gate circuit, said storage circuit being composed of transistors having threshold voltage higher than that of said first transistor,

said second and third transistors being controlled to be OFF when said storage circuit holds said output logic of said gate circuit, and said second and third transistors being controlled to be ON when said storage circuit does not hold said output logic of said gate circuit, and

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.

17. (Original) A flip flop comprising:

a first conduction interception circuit capable of switching conduction or shutoff between an input terminal and an output terminal;

a first storage circuit capable of holding output logic of said first conduction interception circuit;

a second conduction interception circuit which is capable of switching conduction or shutoff between an input terminal and an output terminal and has said input terminal being connected to an output terminal of said first storage circuit; and

a second storage circuit capable of holding output logic of said second conduction interception circuit,

said first and second conduction interception circuits being constituted by said logic operation circuits defined in claim 11,

said first and second storage circuits being constituted by transistors having a threshold voltage higher than those of said gate circuits in said first and second conduction interception circuits.
